AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-24 (canceled)

25. (previously presented) A system semiconductor device, comprising:

a system LSI cell portion which includes a plurality of functional blocks for realizing specific functions, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip; and

a global wiring layer which at least has conductor means formed in a substrate and a wiring layer of a single-layer or a multi-layer structure formed on the conductor means and which is laminated with the system LSI cell portion so that the functional blocks are electrically connected to each other.

26. (previously presented) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has a varied via as the conductor means formed in the semiconductor substrate, a first wiring layer formed on the buried via, an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer and electrically connected to the first wiring layer through the via, and an adhesive layer formed on the insulating layer in an area where the second wiring layer is not formed.

27. (previously presented) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has a buried via as the conductor means formed in the semiconductor substrate, a first wiring layer formed on the buried via, an insulating layer formed on the first wiring layer, a second wiring layer formed on the insulating layer and electrically connected to the first wiring layer through the via, and an inner bump formed on a surface of the second wiring layer.

28. (previously presented) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has a secondary wiring layer as the conductor means formed in the substrate made of an organic material, a first wiring layer formed on the secondary wiring layer, an insulating layer formed on the first wiring layer, a second wiring layer formed on the insulating layer and electrically connected to the first wiring layer through a via, and an adhesive layer formed on the

insulating layer in an area where the second wiring layer is not formed.

29. (previously presented) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has a secondary wiring layer as the conductor means formed in the substrate made of an organic material, a first wiring layer formed on the secondary wiring layer, an insulating layer formed on the first wiring layer, a second wiring layer formed on the insulating layer and electrically connected to the first wiring layer through the via, and an inner bump formed on a surface of the second wiring layer.

30. (previously presented) A system semiconductor device as claimed in claim 27, wherein a gap is present between the global wiring layer and a circuit surface of the LSI cell portion connected by the inner bump.

31. (previously presented) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has a bump which is arranged on a substrate surface on the side where the wiring layer is not formed and which is adapted to be

electrically connected to an external circuit through the conductor means.

32. (previously presented) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has one or more wiring layers as the wiring layer.

33. (previously presented) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has one or more insulating layers as the insulating layer.

34. (previously presented) A system semiconductor device as claimed in claim 25, wherein:

a plurality of the system LSI cell portions are formed on a semiconductor wafer;

a plurality of the global wiring layers are formed on the semiconductor substrate; and

the semiconductor wafer and the semiconductor substrate are laminated, diced and separated to obtain a plurality of the system semiconductor devices.

35-44. (canceled)

45. (previously presented) A system semiconductor device as claimed in claim 29, wherein a gap is present between the global wiring layer and a circuit surface of the LSI cell portion connected by the inner bump.

46. (canceled)

47. (previously presented) A system semiconductor device, comprising:

a system LSI cell portion which includes a plurality of functional blocks for realizing specific functions and which has pads formed on the functional blocks, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip; and

a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other;

the global wiring layer comprises;

a first wiring layer formed on the semiconductor substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer,

a first via which is formed in the insulating layer and which electrically connects the first wiring layer with the second wiring layer, and

a second via which is buried in the semiconductor substrate and which is electrically connected to the first wiring layer and which serves as en electrode for an external circuit,

the global wiring layer being laminated with the system LSI portion by electrically connecting the functional blocks with the second wiring layer through the pads so that the functional blocks are electrically connected to the external circuit through the first wiring layer and the second wiring layer.